

DRAWINGS
FOR
APPLICATION
FOR
UNITED STATES LETTERS PATENT

TITLE: TRANSMITTING MPEG DATA PACKETS RECEIVED
FROM A NON-CONSTANT DELAY NETWORK

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FIGURES: 1 through 4

SHEETS: 4

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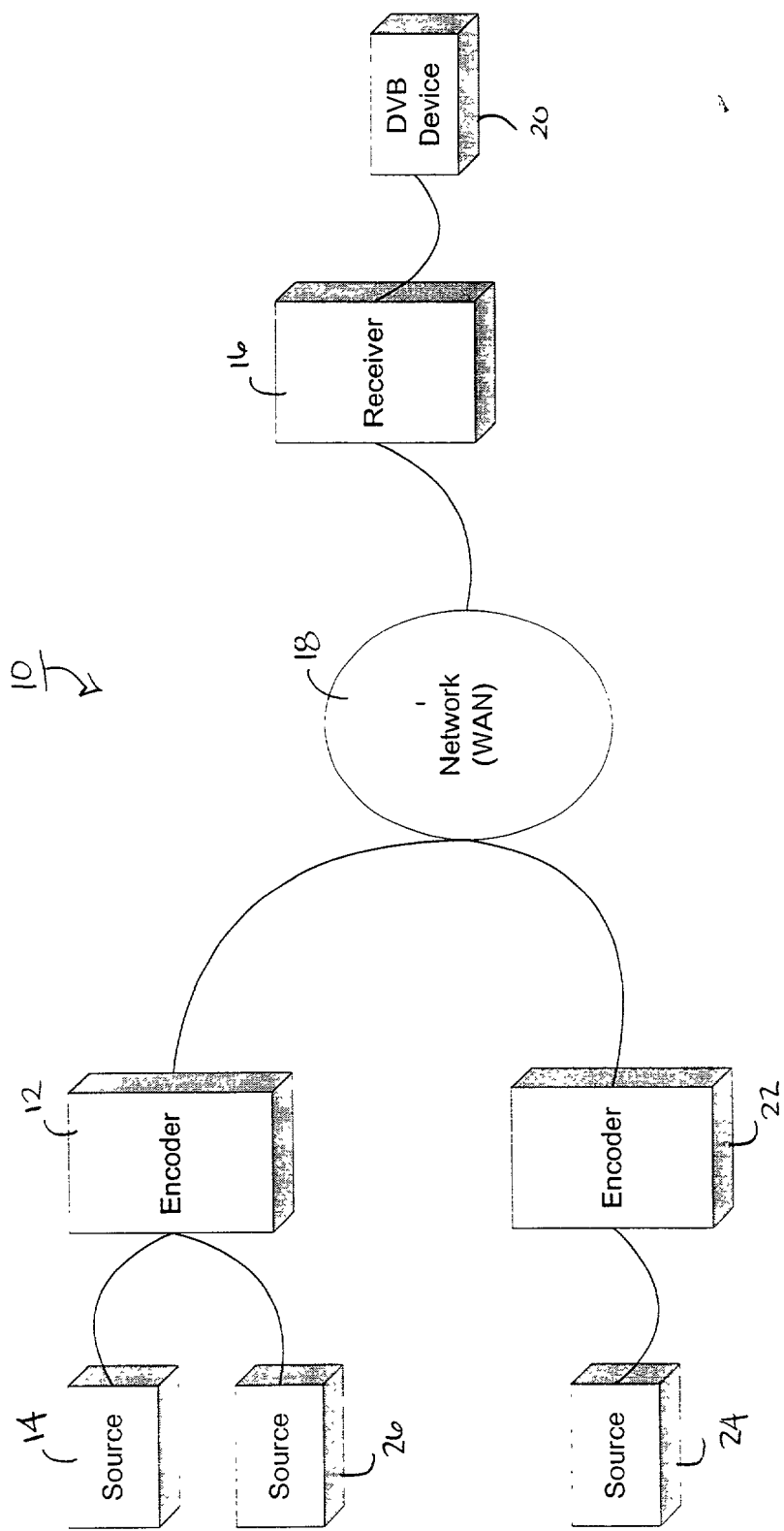


FIG. 1

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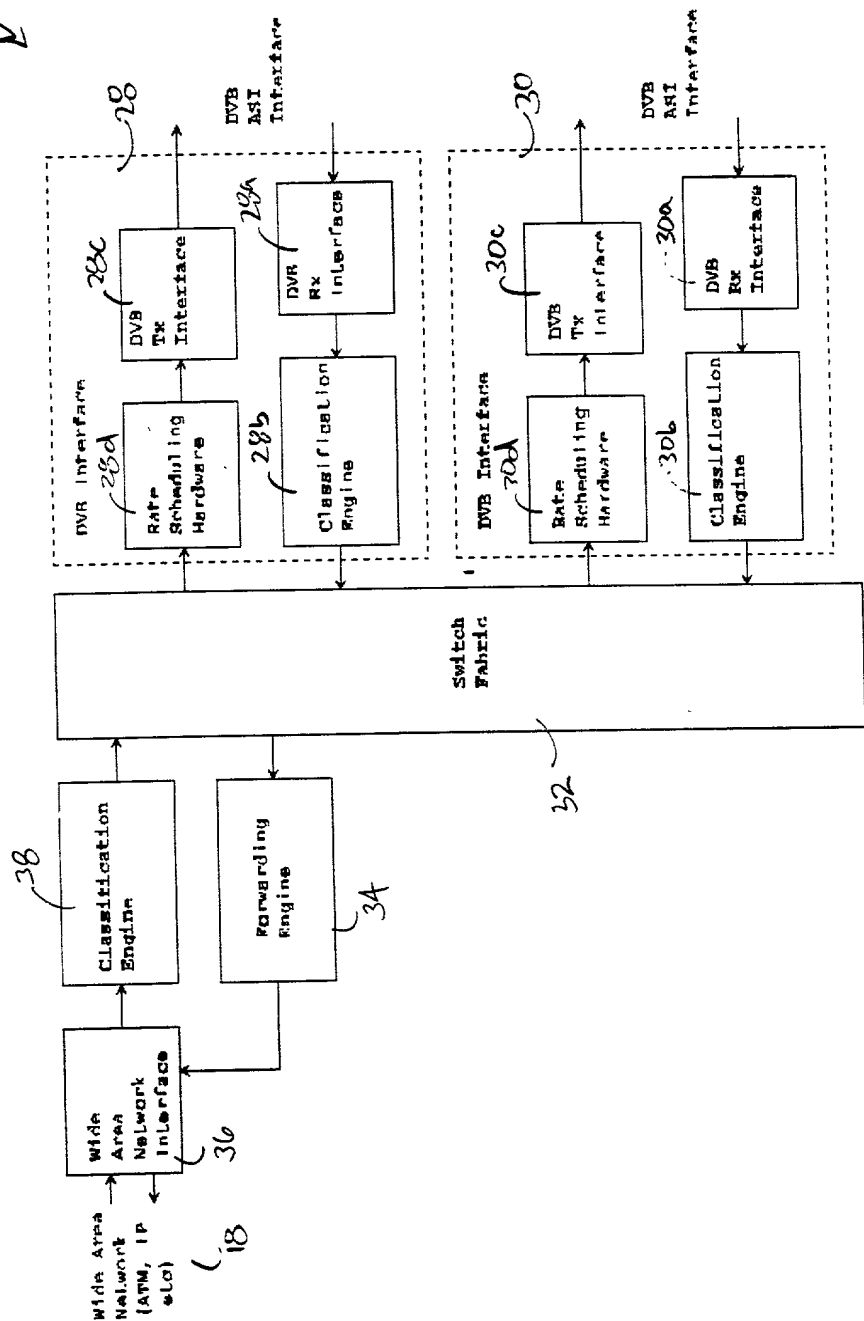


FIG. 2

FIG. 3 is a block diagram of a system architecture for a video-on-demand (VOD) system. The system includes a Main Processor (94) and Main Memory (96) connected to a central bus (98). The bus (98) is connected to various components including a Bus Switch FIFO (104), a Queueing Dual Port RAM (44), a Video Input/Output Controller (68), a Video Input/Output Controller (66), a Video Input/Output Controller (64), a Video Input/Output Controller (62), a Video Input/Output Controller (60), a Video Input/Output Controller (58), a Video Input/Output Controller (56), a Video Input/Output Controller (54), a Video Input/Output Controller (52), a Video Input/Output Controller (50), a Video Input/Output Controller (48), a Video Input/Output Controller (46), a Video Input/Output Controller (44), a Video Input/Output Controller (42), a Video Input/Output Controller (40), a Video Input/Output Controller (38), a Video Input/Output Controller (36), a Video Input/Output Controller (34), a Video Input/Output Controller (32), a Video Input/Output Controller (30), a Video Input/Output Controller (28), a Video Input/Output Controller (26), a Video Input/Output Controller (24), a Video Input/Output Controller (22), a Video Input/Output Controller (20), a Video Input/Output Controller (18), a Video Input/Output Controller (16), a Video Input/Output Controller (14), a Video Input/Output Controller (12), a Video Input/Output Controller (10), a Video Input/Output Controller (8), a Video Input/Output Controller (6), a Video Input/Output Controller (4), a Video Input/Output Controller (2), a Video Input/Output Controller (0).

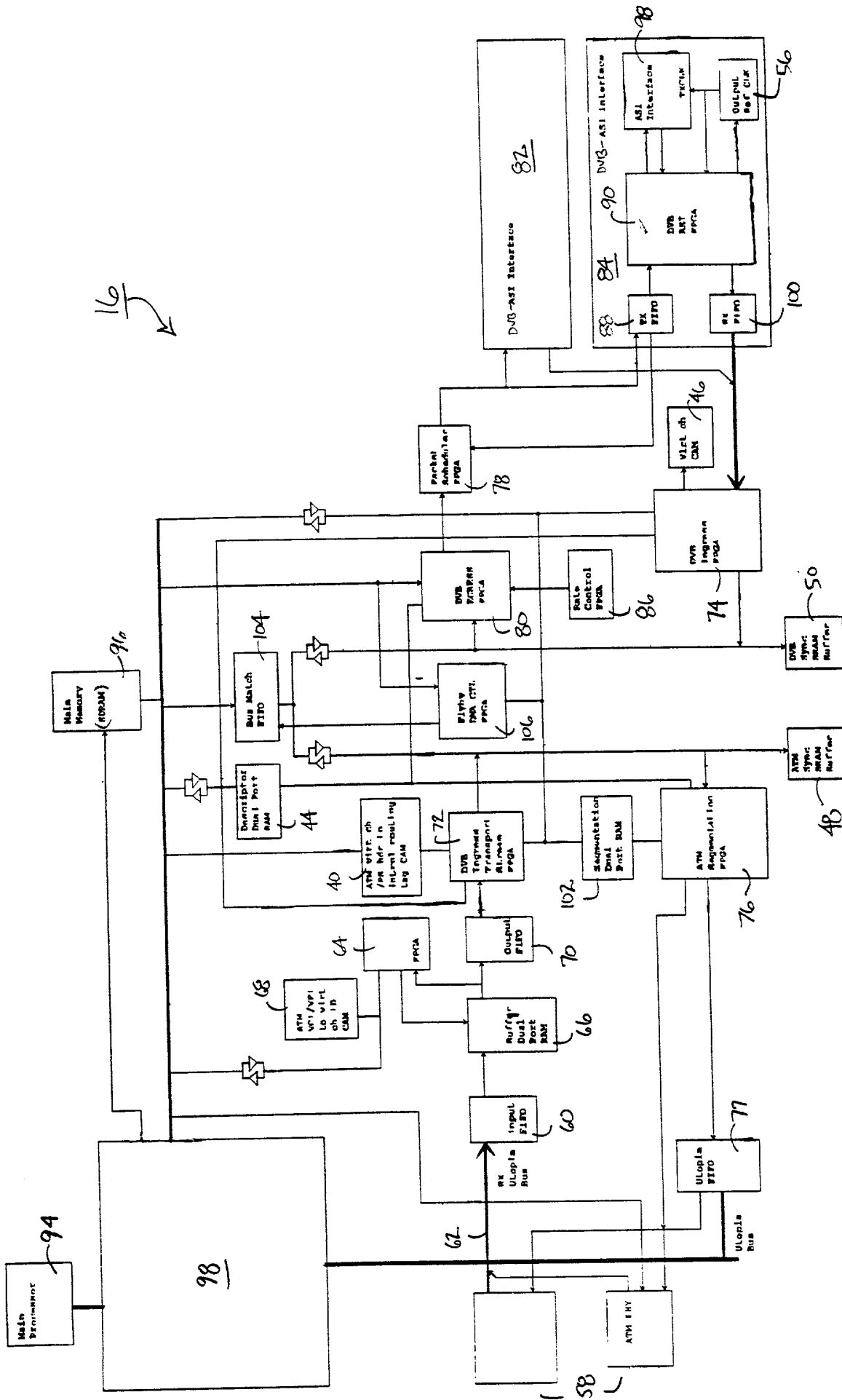


FIG. 3

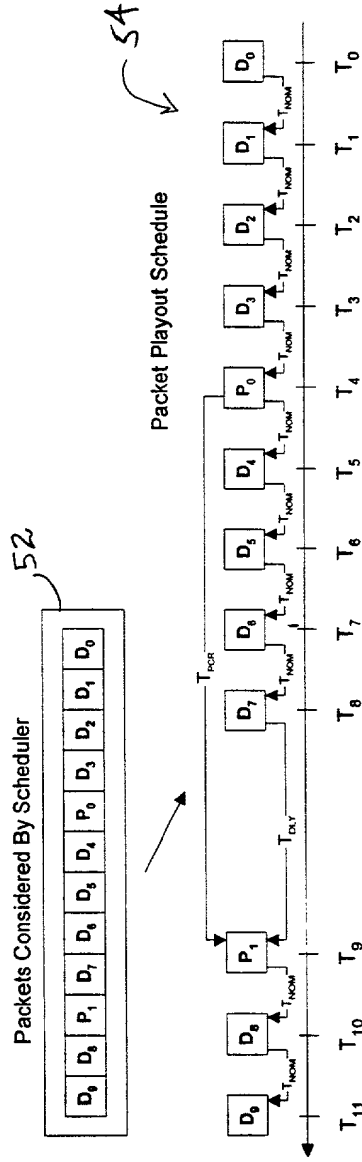


FIG. 4